Fast orbit feedback in a mixed BPM environment

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DELTA Parameters:

Beam energy: 550 MeV – 1.5 GeV
Beam current: 120 mA @ 1.5 GeV
Beam lifetime: 8 h @ 100 mA
Availability: > 90 %
Operational: 3000 h / year

Personnel:

2 Professors
4 Accelerator physicists
2 Beamline scientists
1 Administration
8 Technicians
X Students

Why a fast orbit feedback?

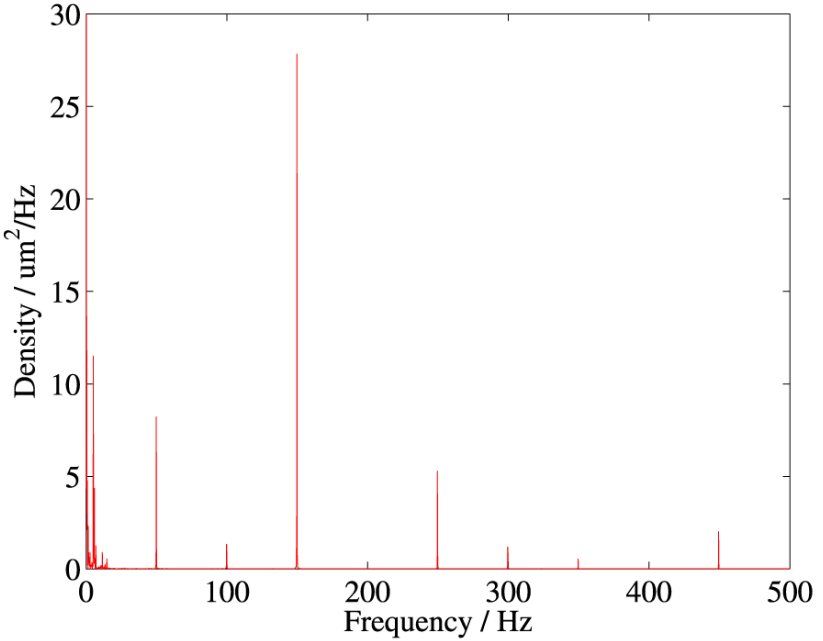
- Compensate for low frequency girder movement

- Compensate for 50/150/250 Hz beam movement

- Compensate for ID movement

- Compensate for BoDo ramp influence on Delta orbit

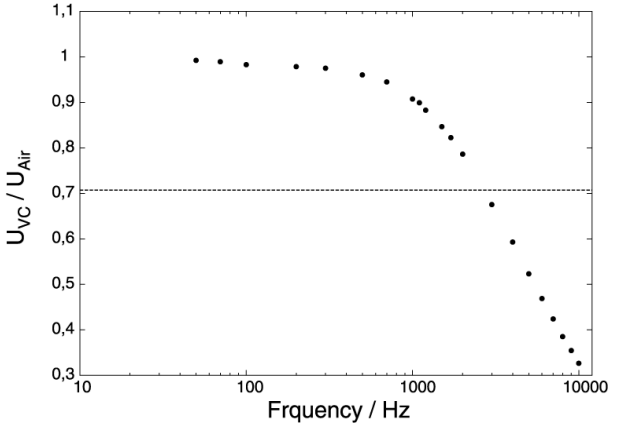
- Stabilize FEL operation (at low beam currents)



Limitations:

- Magnet inductance

- Vacuum chamber eddy currents



=> Bandwidth limit at about 1 kHz with correctors 'ex vacuum'

Cost estimate for a global orbit feedback:

Using Liberas only:		**Using Liberas & available Bergoz MX-BPMs**	
44 additional Liberas	450 k€	11 XUP boards+ADC	5 k€
40 Correctors	4 k€	40 Correctors	4 k€
40 Corrector PS	80 k€	40 Corrector PS	80 k€
Additional Hardware	4 k€	Additional Hardware	4 k€
Sum	**538 k€**	**Sum**	**93 k€**

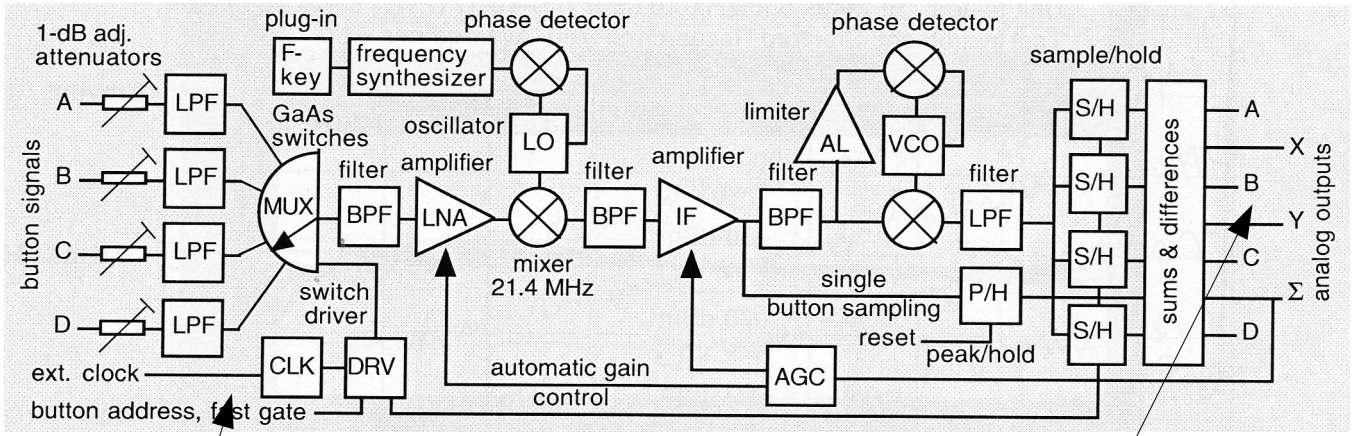
But: XUP board must be programmed to make 4 Bergoz BPMs look like 4 Liberas.

First step: Setup of a fast local orbit feedback using 2 BPMs and 4 new correctors

Drawbacks:

- Delta's slow corrector magnets on quadrupole yokes can't be used
  (Inductance: 200 mH, would need 600V driver voltage)

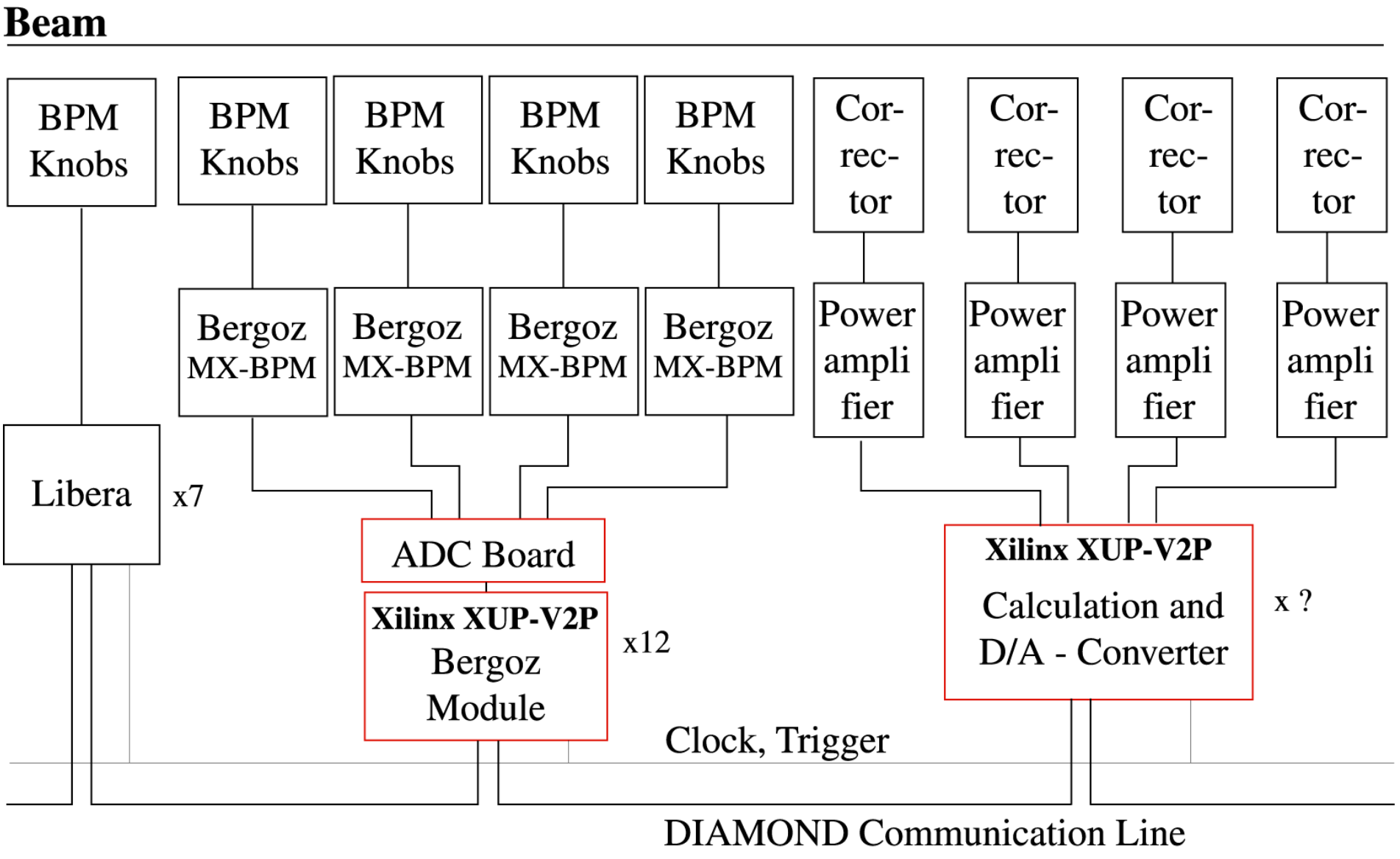
MX BPMs:



External clock up to 40 kHz

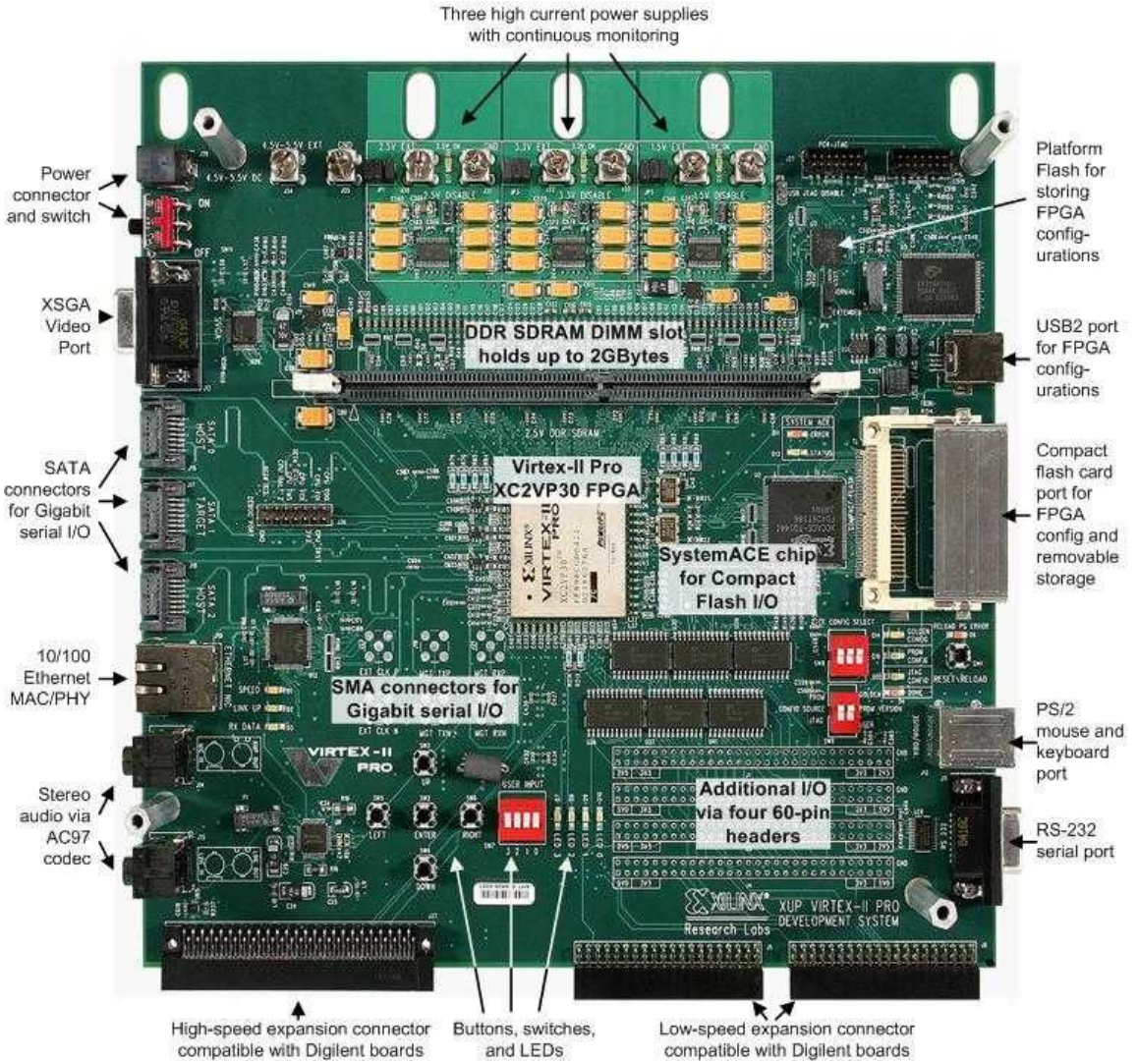
Max. data rate 10 kHz

Delta's future fast global orbit feedback



XUP Virtex II Pro board

- Same FPGA as in Liberas
- All peripherals included
- Inexpensive



ADC Board

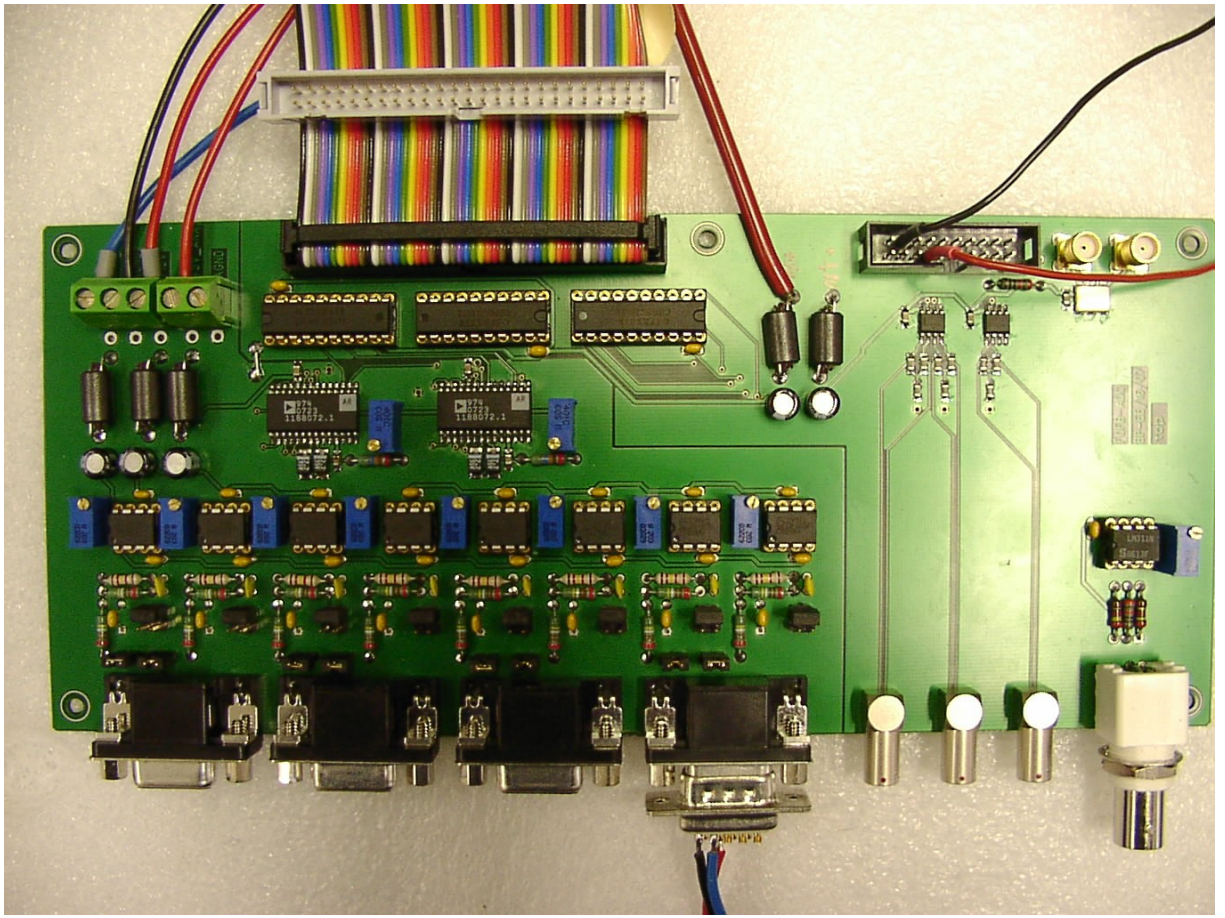
- 2 ADC's
  - 4 channel
  - 200kS/s

- Low pass filters on input (optional)

- Buffered bus

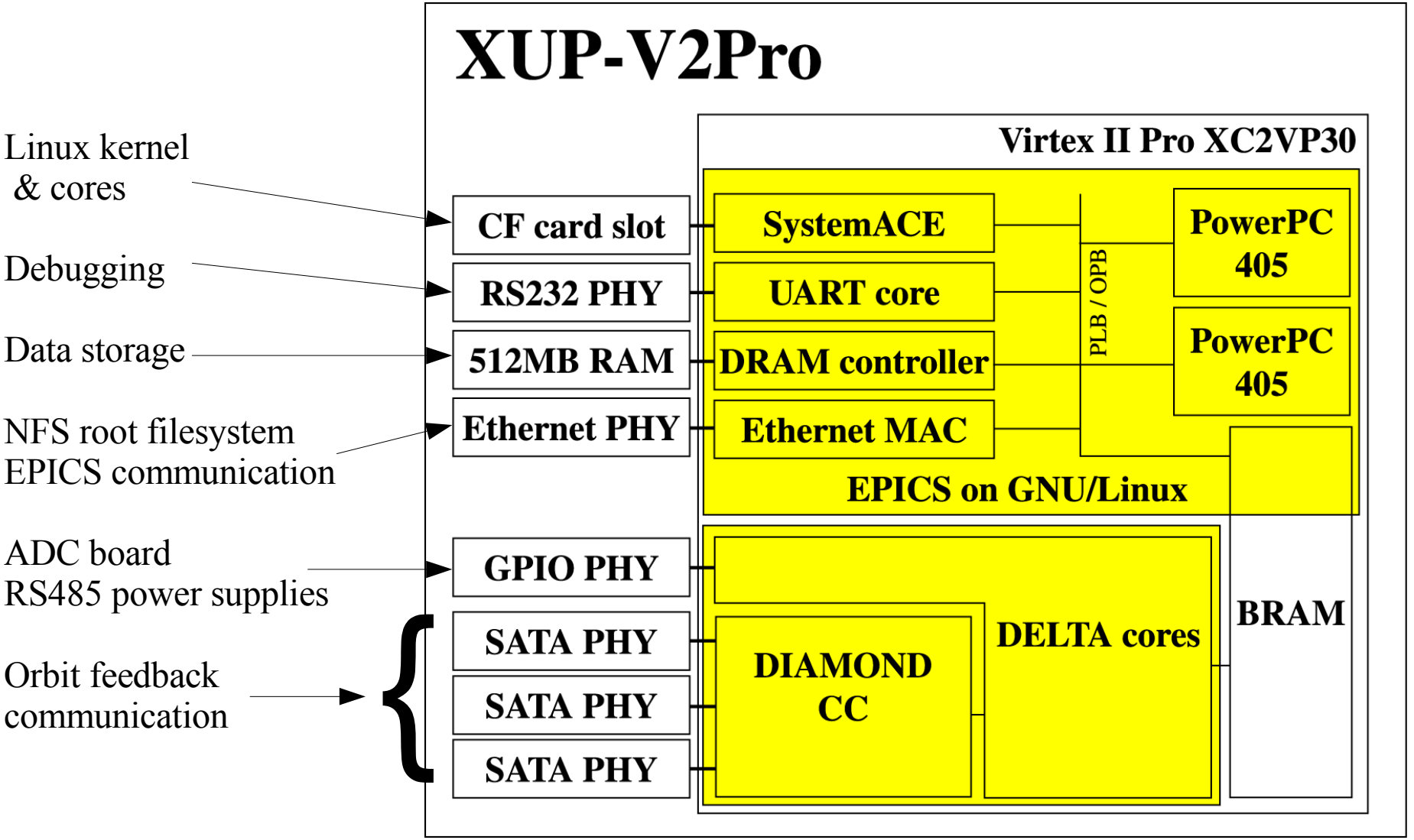
- 106.25 Mhz clock

- Signal ports (clock splitter)
  - Trigger
  - Machine clock
  - System clock



A well synchronized system will sample each signal at 50kS/s.

XUP Board setup for DELTA



Project status:

General:

Run GNU/Linux on XUP-board - done
Run EPICS/SoftIOC on XUP-board - done
Establish communication EPICS <-> Delta cores through OPB/BRAM - pending
Implement EPICS driver for BRAM – pending

BPM-XUP:

Implement DIAMOND CC on XUP-boards - done
Establish communication XUP <-> XUP - done
Design ADC board - done
Read/write data from/to ADC board - done
Synchronize the four Bergoz BPMs - done
Design XUP fiber transceiver for long distance communication - pending
Setup communication btw. XUP-board and Liberas - pending
Synchronize to master bus clock - pending

Local orbit feedback-XUP:

Buy fast power supply for Delta correctors – done
Set up corrector magnets for local feedback – done
Measure frequency limit of vacuum chamber – done
Implement DIAMOND CC on Liberas - pending
Implement & test UART cores for corrector power supplies - pending
Implement data processing algorithms – pending

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FPGA Implementation details:
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The I-Tech team

The DELTA team