ALBA
SYNCHROTRON LIGHT SOURCE

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Título puesto: Modeling an RF cavity with digital electronics
Curso: 2025/26
División: Aceleradores/Computing

Descripción del proyecto:

At the ALBA Synchrotron, RF cavities are used to accelerate electron beams or maintain their current energy. These cavities are fed by high-power radio-frequency electromagnetic waves to build up a high axial electric field.

Digital Low-Level RF (LLRF) systems are responsible for driving the RF amplifiers of these cavities and stabilizing their internal electromagnetic fields. The core component of a Digital LLRF system is an FPGA, which analyzes signals from the cavities and generates control signals for the RF amplifiers.

Whenever a new feature is added to the LLRF system, an intermediate test must be conducted before performing the final test on the RF cavities with the beam. To enable this, a virtual RF cavity must be implemented in the FPGA as an HDL module. This requires translating the established mathematical model of the RF cavity into MATLAB/Simulink, converting it to a fixed-point model, and then writing HDL code (VHDL or Verilog) for FPGA implementation.

The student can begin by developing a simplified RF cavity model, with additional capabilities gradually incorporated later under the mentor's guidance.

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Perfil del estudiante:

Student Profile: Physics, Electrical Engineering, or related engineering discipline.

Requirements:

- Basic knowledge of **electromagnetics** and **high-frequency RF theory**.
- Familiarity with **programming tools** such as MATLAB/Simulink or Python.
- Basic understanding of **FPGA architecture** and **HDL languages** (VHDL or Verilog).
- Introductory experience with **digital signal processing (DSP)** concepts.
- Good level of **spoken and written English**.

Program:

- **Introduction to Low-Level RF Systems**: Overview of their role in particle accelerators.
- **RF Cavity Modeling**: Principles, mathematical foundations, and simulation techniques.
- **Fixed-Point Implementation**: Translating RF cavity models to MATLAB/Simulink (or Python), converting to fixed-point arithmetic, and testing via HDL (VHDL/Verilog).
- **Project Documentation**: Compiling technical reports, code comments, and validation results.

Tutor: Hamed Shaker

Responsable División: Francis Pérez