# Digital LLRF system for the SOLEIL Upgrade and LUCRECE projects

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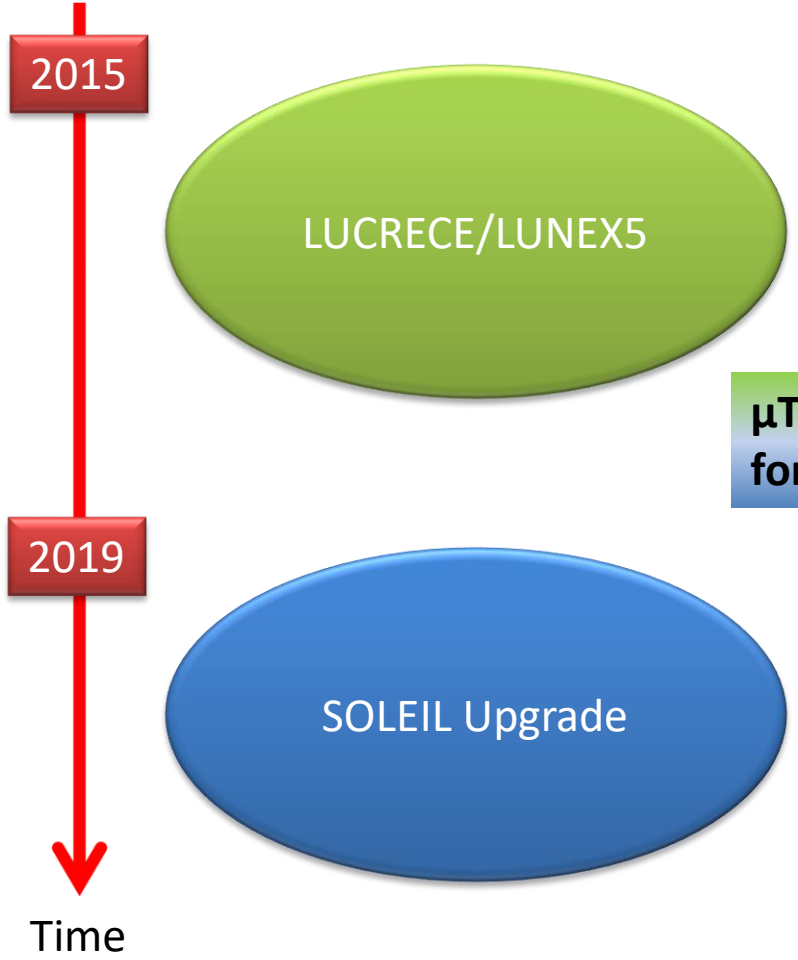
# Digital µTCA.4 platform




**µTCA.4 platform and Zynq for DLLRF system**

**LUCRECE**:
Program of R&D about RF technology for CW Linacs, with the aim to LUNEX5

**Soleil upgrade**:
P. Marchand's presentation
« RF SYSTEMS FOR THE SOLEIL UPGRADE RESULTS OF STUDIES FOR THE CDR »

# LUCRECE project

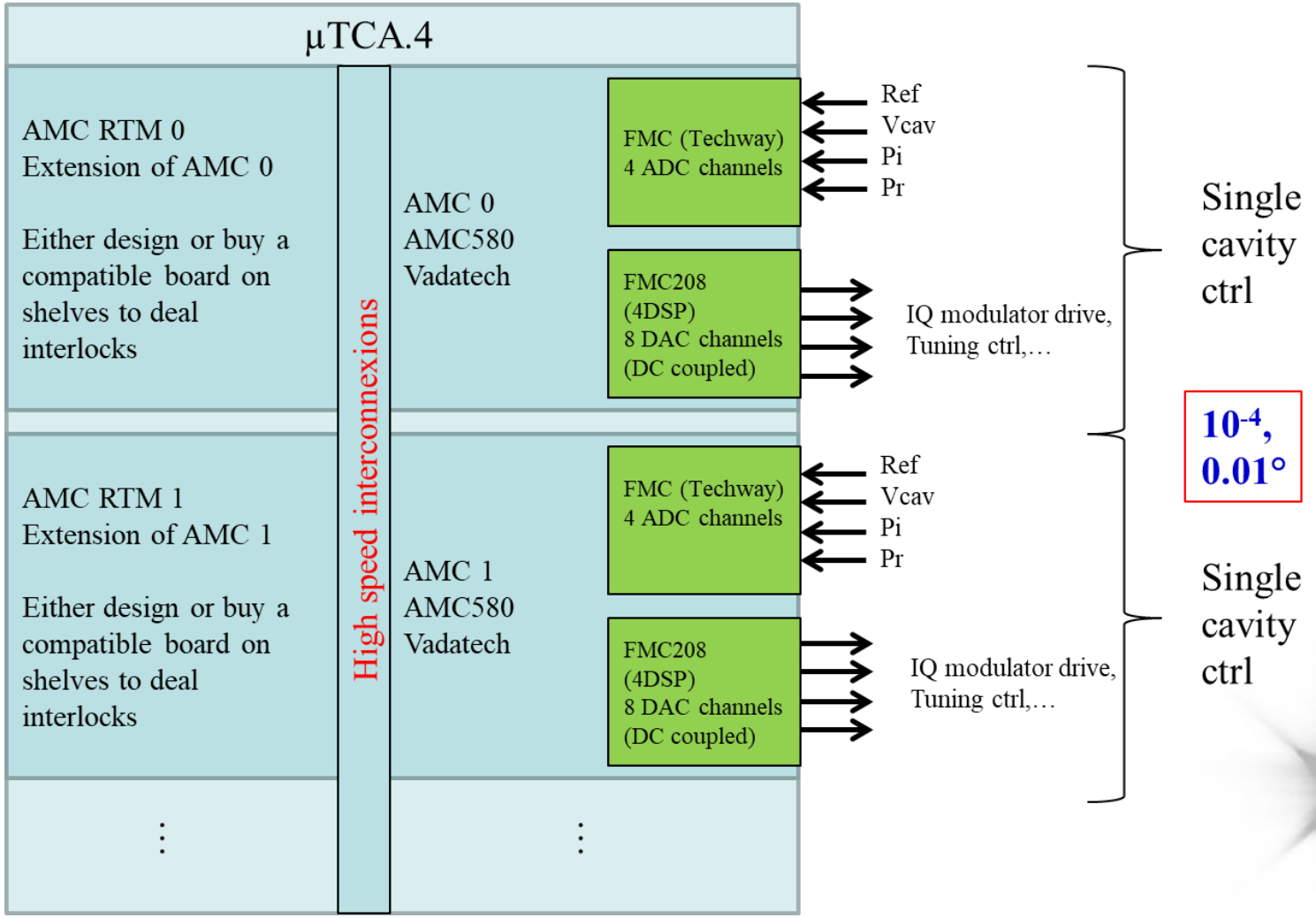
- It takes place in the context of the LUNEX5 (free electron Laser Using a New accelerator for the Exploitation of X-ray radiation of 5th generation) advanced and compact FEL demonstrator, using superconducting linac technology for high repetition rate and multi-user operation.

- The LUCRECE project aims at developing an elementary RF system (cavity, power source, LLRF and controls) suitable for continuous (CW) operation at 1.3 GHz in Energy Recovery Linacs (ERL) and VUV-X-ray femtosecond free electron laser (FEL) based light sources at high repetition rate.

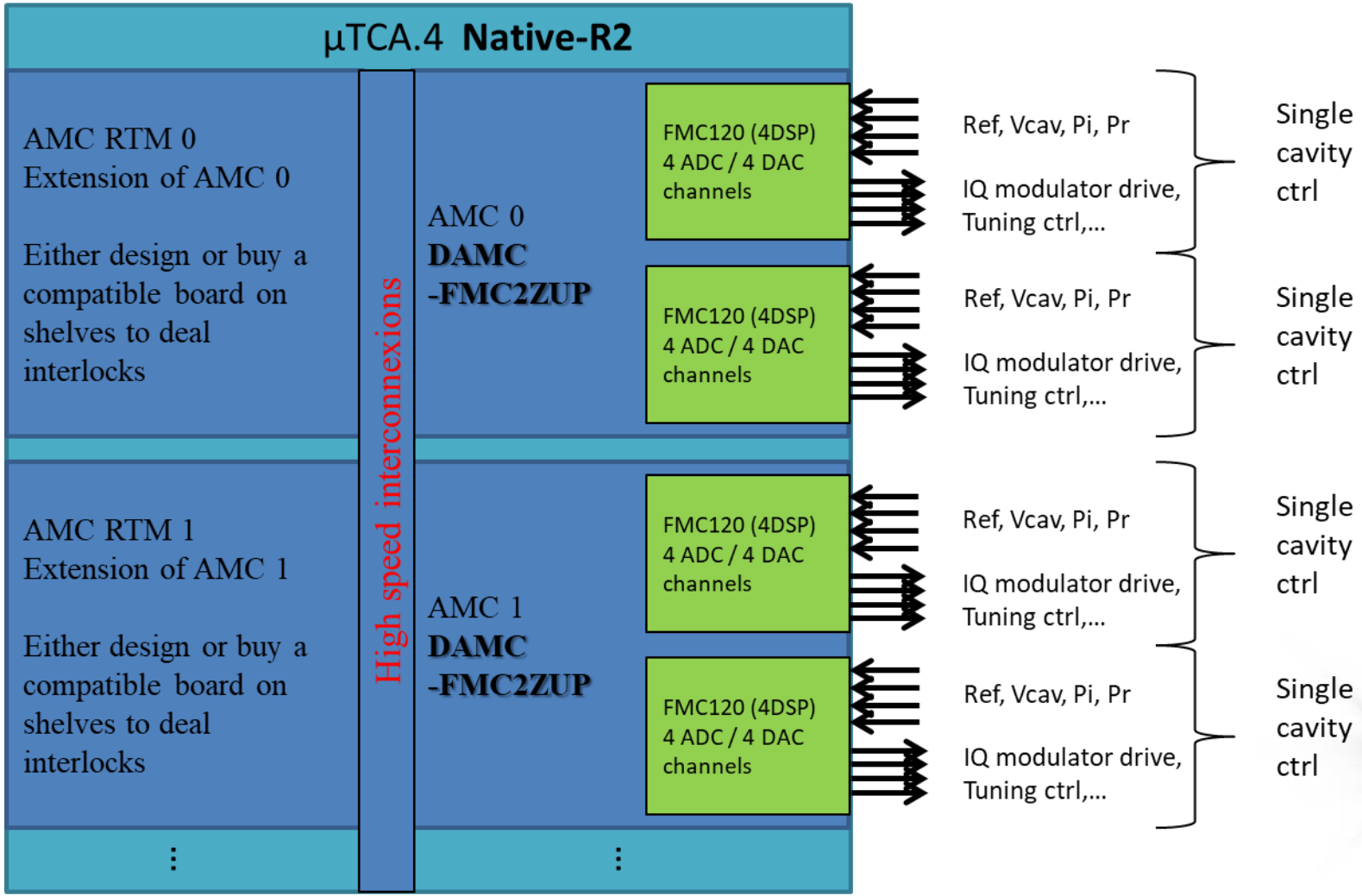
- A 1.3 GHz superconducting accelerating structure and its related components (tuner, fundamental and HOM couplers, Helium manifold, etc.) will be designed for CW operation.

- The SOLEIL LLRF team is in charge of developing a µTCA based digital LLRF prototype.

# D-LLRF architecture for LUCRECE



# D-LLRF architecture for Soleil Upgrade



# Vadatech solution

List of Materials (µTCA):

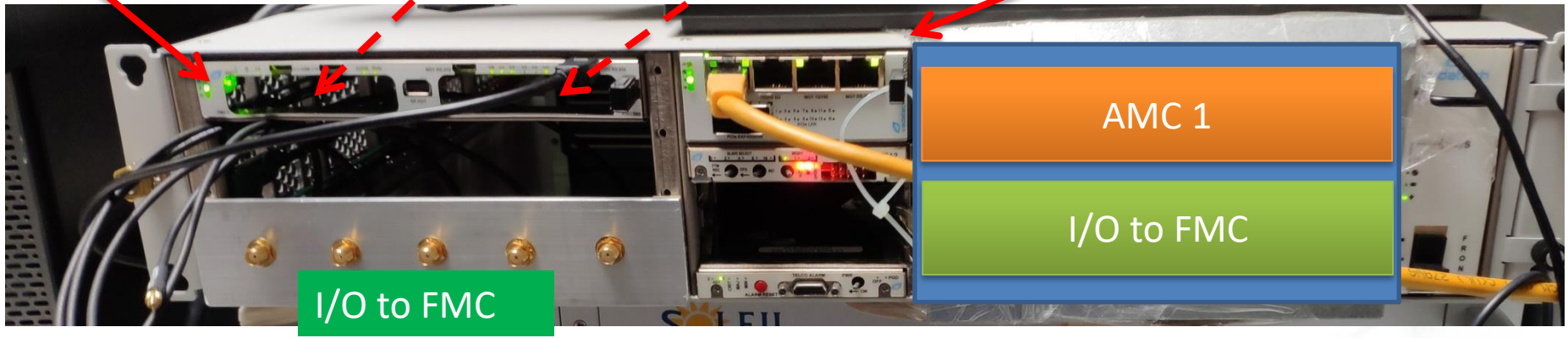
- AMC580:  Xilinx Zynq Ultrascale+ MPSoC XCZU19EG FFVC1760 FPGA
- FMC224+FMC120: DAC+ADC
- UTC004: MCH
- VT812: µTCA.4 chassis

MCH UTC004

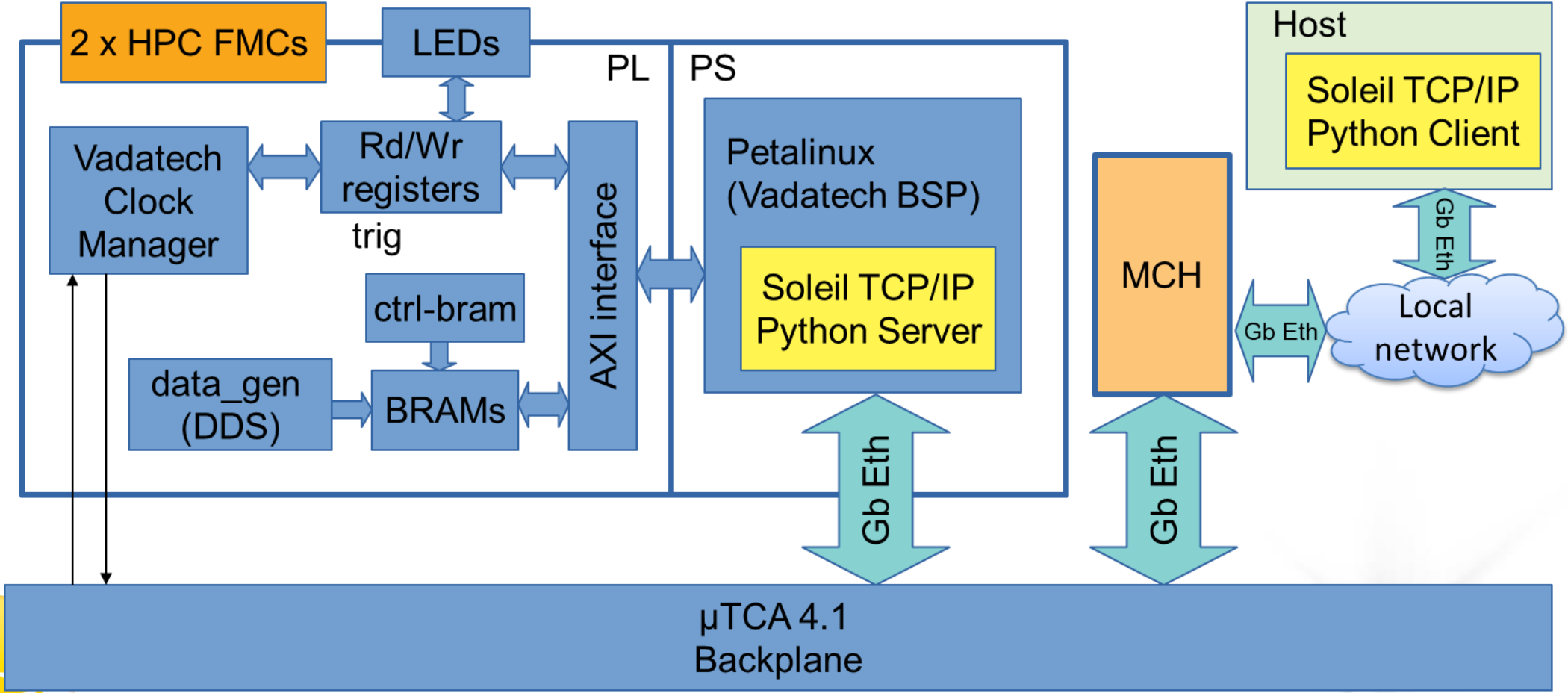
FMC_ADC_4CH_125

FMC224

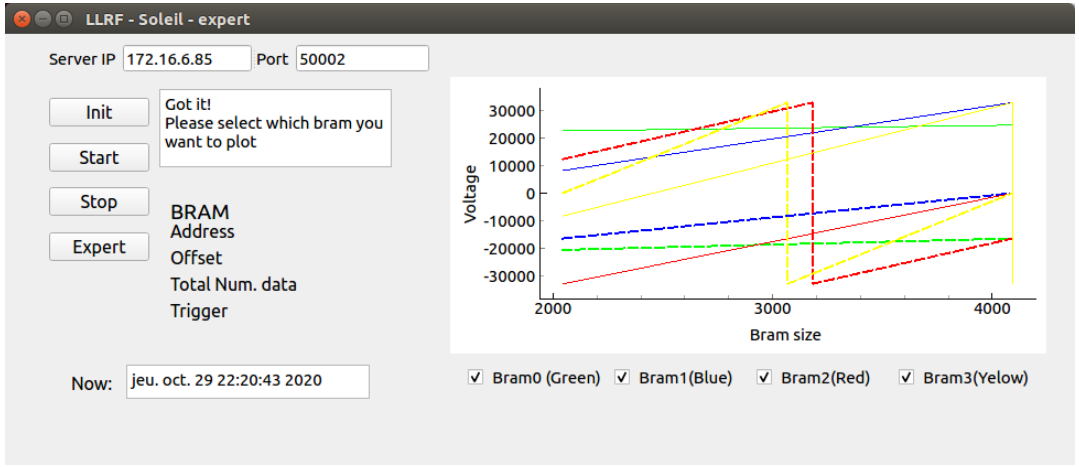
AMC580

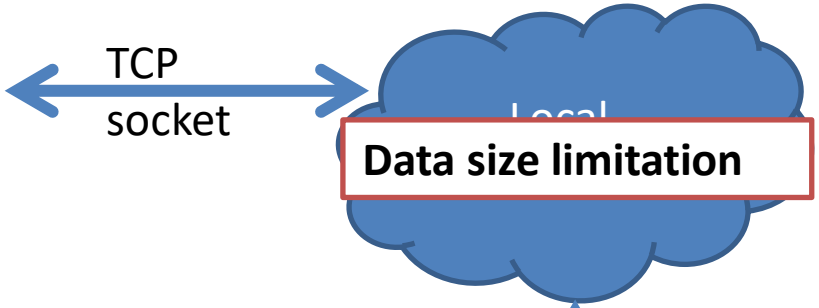


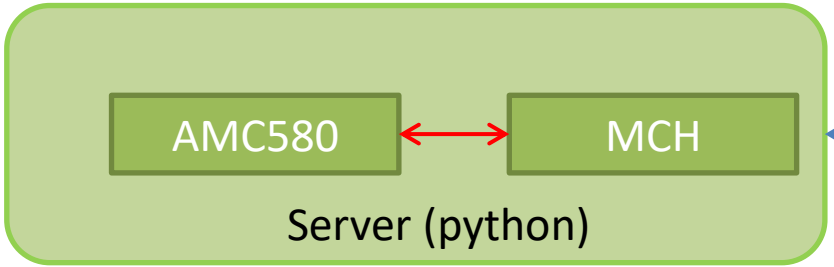
# Vadatech solution

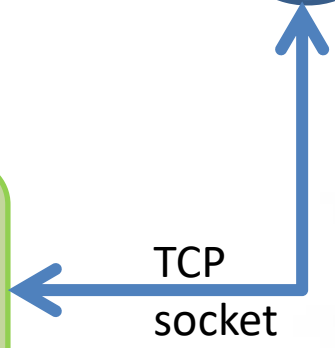


Client(python)



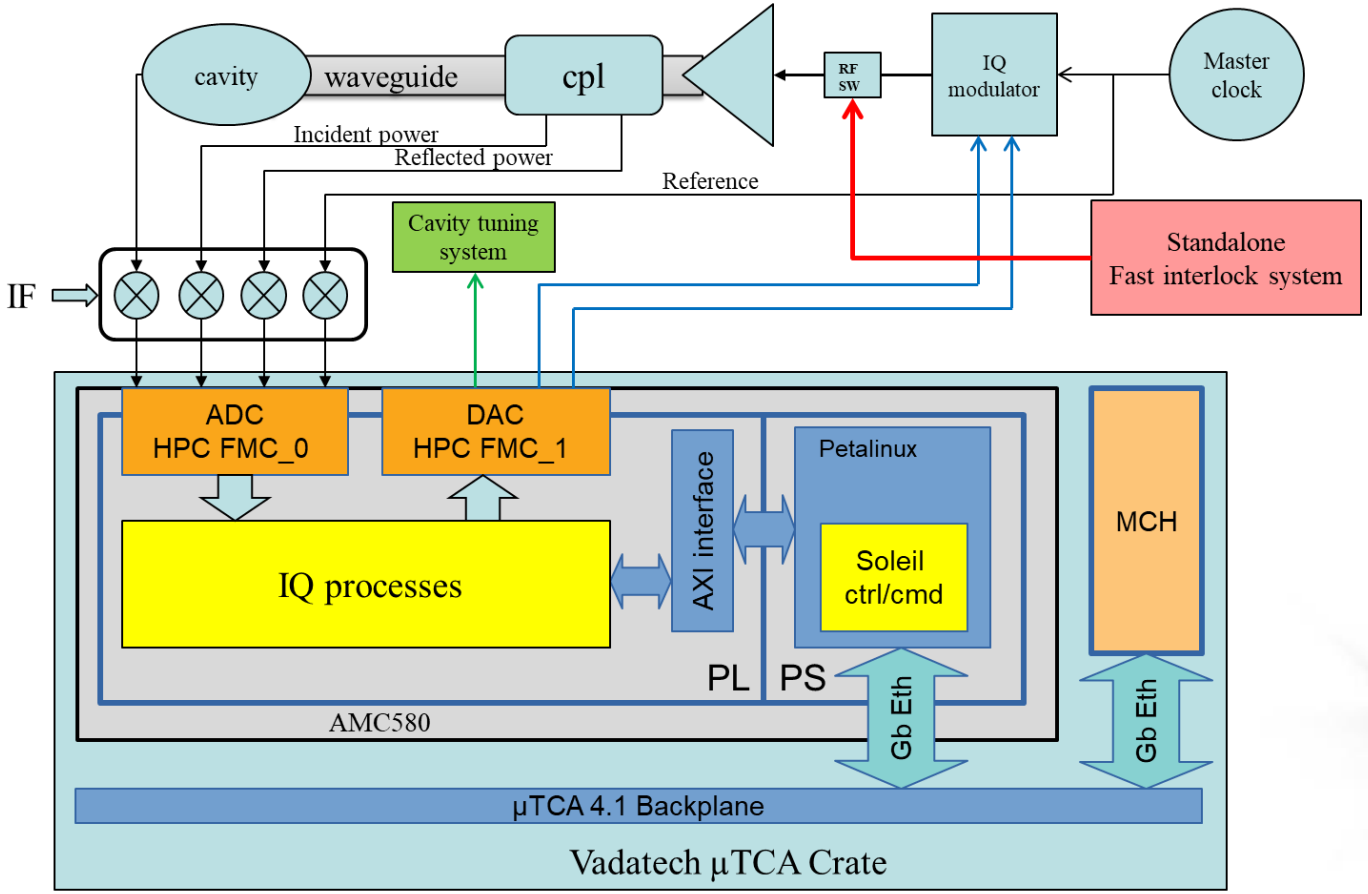



# 352 MHZ LLRF SYSTEMS

✓A generic digital version, based on µTCA /Zynq environment, is being developed for our LUCRECE project at 1.3 GHz, which will be easily adapted for SOLEIL-U.



# NAT solution

- **µTCA Native-R2 MCH-PHYS80**

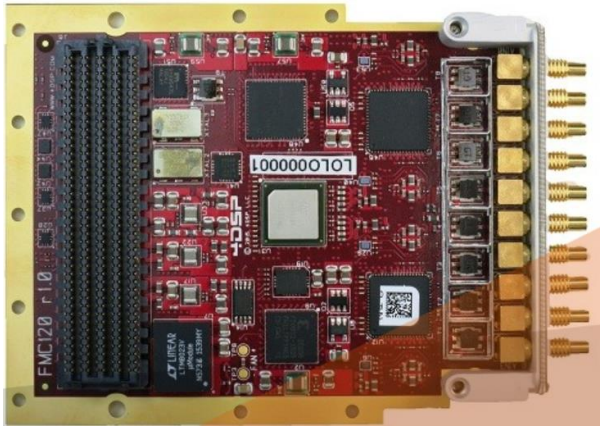
  - ✓ six horizontally-mounted AMC modules (five mid-size and one full-size),
  - ✓ up to five MicroRTMs (uRTM), and
  - ✓ one JTAG switch module (JSM).

- **DAMC-FMC2ZUP**

delivery date: ~01/2021

  - ✓ FPGA Low-Power Xilinx UltraScale+ MPSoC XCZU11EG-L2FFVC1760E
  - ✓ The board also provides a front panel connector with Gigabit Ethernet interface (over a SFP+), clock input and two trigger IN/OUT signals
  - ✓ The DAMC-FMC2ZUP is supported by all modern development tools as Vivado, HLS, Yocto, Petalinux, SDSoC and SDAccel

# FMC 120




The FMC120 provides four 16-bit A/D channels up to 1Gsps, four 16-bit D/A channels up to 1.25Gsps and up to 2.8Gsps sample rate with interpolation. The devices can function up to 1Gsps during simultaneously D/A and A/D operation as the clock source is shared.

- The design is based on Texas Instruments' ADS54J60 Analog-to-Digital converter and Texas Instruments' DAC39J84 Digital-to-Analog converter.
- The sample clock can be supplied externally through a coax connection or supplied by an internal clock source (optionally locked to an external reference). Additionally, a trigger input is available for customized synchronization.
- When paired with the latest FPGA carrier cards such as the 4DSP VP868 with Xilinx Ultrascale technology, customers can innovate high performance algorithms on an industry standard platform.

# Summary

**DLLRF at Soleil:**

- Exploring Zynq ultrascale +
  - ✓ Communication between CPU and FPGA
  - ✓ Read data from BRAM via network
- To do :
  - ❑ FMC ADC from TECHWAY
  - ❑ FMC DAC from vadatech
  - ❑ Custom BSP image

- Simulation Simulink/Matlab
  - PI and time delay etc.

# Thanks

# FMC Techway


Analog to digital converters FMC @ 125 MSPS

ADC125 is a fully compliant FMC mezzanine (VITA 57.1) which offer 4 16 bits A/D channels up to 125 MSPS. ADC125 FMC is based on 2 dual Analog-to-Digital converters from Linear Technology : the LTC2185.

Fine-tune the ADCs through the $I^2C$ bus. ADC gain, bias and delay

# FMC 224 Vadatech

The FMC224 is an FPGA Mezzanine Card (FMC) per the VITA 57 specification. The module has a quad Port DAC 16-bit @ 2.8 GSPS.

The DAC converter utilizes the TI DAC39J84 which is JESD204B compliant. The device includes features that streamline the design of complex transmit architecture. It includes fully by-passable 2x to 16x digital interpolation filters with over 90 dB of stop-band attenuation to simplify the data interface.
An on-chip 48-bit Numerically Controlled Oscillator (NCO) and independent complex mixer allow flexible and accurate carrier placement.
The module has a wide-band PLL which can take its reference clock via the front panel, FMC Carrier or the onboard reference. The unit also allows the RF Clock syntheses to be generated by the onboard wide-band PLL or the front panel.